REMARKS

Reconsideration of this application as amended is respectfully requested.

In the Office Action dated January 4, 2006, claims 1, 4-9, 12-17 and 20-24 were pending. Claims 1, 4-9, 12-17 and 20-24 were rejected. In this response, claims 1, 4-9, 12-17 and 20-24 remain pending. Claims 1, 9 and 17 have been amended. No claims are added. No claims are canceled. Support for the amendments can be found throughout the specification as filed. However, Applicant specifically directs Examiner's attention to lines 10-15, page 12. No new matter has been added.

Amendments

Rejections under 35 U.S.C. § 103(a)

Claims **1, 4-9, 12-17 and 20-24**

Claims 1, 4-9, 12-17 and 20-24 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Andrew et al., U.S. Patent No. 5,428,403 (hereinafter "Andrew") in view of Akiwumi-Assani et al., U.S. Patent No. 5,532,744 (hereinafter "Akiwumi-Assani"). However, Applicant respectfully submits that Applicant's invention as claimed in claims 1, 4-9, 12-17 and 20-24, as amended, is patentable over the cited references.

Specifically, for example, independent claim 1, as amended, includes:

> "assigning, via a first processor of a group of symmetric multiple processors sharing said memory, at least one independent slice per processor to be decoded by the processors in parallel, including assigning a varying number of slices to individual processors; and
> each of the symmetric multiple processors, including the first processor, decoding the assigned slices in parallel without reading from a program memory other than the shared memory."
> (emphasis added)

Applicant's amended claim 1 contains the limitations that one of a group of symmetric multiple processors assigns at least one slice to each processor, including the assigning processor, a slice to decode in parallel, the group of symmetric multiple processors reading programs from a shared

memory. It is respectfully submitted that the above limitations are absent from both Andrew and Akiwumi-Assani, individually or in combination.

Andrew teaches a method of estimating a motion vector for a given block of pixels in a frame of a digitized motion picture sequence using a system of four parallel digital signal processors (Andrew, col. 3, lines 30-35, col. 6, lines 35-41). The method is described to encode digitized video images. Each digital signal processor has a pair of program memories. The program for the digital signal processor is stored in one of the program memories. (Andrew, col. 6, lines 66-68). A memory for the storage of the video data frames being encoded is connected to the digital signal processors through a high speed bus (Andrew, col. 6, lines 45-55). Indeed, each digital signal processor houses its own program instance while accessing the common input video data. Hence, the digital signal processor is not a symmetric multiprocessor. Nowhere in Andrew discloses or suggests one of a group of symmetric multiple processors assigns at least one slice to each processor, including the assigning processor, a slice to decode in parallel, the group of symmetric multiple processors reading programs from a shared memory.

Akiwumi-Assani describes a video decoder including a system controller and a plurality of decoder modules. Each decoder module comprises a variable length decoder buffer, a variable length decoder and a decode engine which performs inverse DCT and quantization functions. Examples of decoder design are ICs performing DCT and IDCT functions, ICs performing quantizer and inverse quantizer functions, and digital signal processors (Akiwumi-Assani, col. 4, lines 5-20). It is well known in the art at the time of invention that a digital signal processor has its own program memory. A system controller, which can be programmed by one skilled in digital processing art, detects the start code and determines display parameters following the start code (Akiwumi-Assani, col. 5, lines 1-12). A slice parser **26**, controlled by the system controller **24**, directs bitstream to a decoder module **12**. (Akiwumi-Assani, col. 5, lines 33-63, Fig. 1). Clearly, the processor running the system controller **24**, including the slice parser **26,** is not assigned any slice and does not perform any slice decoding. Nowhere in Akiwumi-Assani discloses or suggests one of a group of symmetric multiple processors assigns at least one slice to each processor, including the assigning processor, a slice to decode in parallel, the group of symmetric multiple processors reading programs from a shared memory.

In contrast, the present invention as claimed includes a set of processors as peers, where one of the peers assigns slices to all peers, including itself, which is absent from the cited references.

Furthermore, Andrew discloses a picture encoding technique to enable improved motion vector estimation to be performed using hardware (Andrew, col. 2, lines 17-20) and to improve generally the encoded motion picture quality (Andrew, col. 3, lines 55-58, col.4, lines 16-18). Akiwumi-Assani, on the other hand, attempts to provide a decoder which can process an output bitstream which is peaky and bursty in an effective and efficient manner (Akiwumi-Assani, col. 2, lines 39-43). However, there are neither suggestions nor motivations in both Andrew and Akiwumi-Assani to combine the references.

As such, not only do Andrew and Akiwumi-Assani not disclose, individually or even in combination, the above noted limitations, but the references, considered as a whole, do not suggest the desirability and thus the obviousness of making the combination.

In order to render a claim obvious, each and every limitation of the claim must be taught by the cited references. Therefore, in view of the foregoing remarks, it is respectfully submitted that independent claims 1, as amended, are patentable over Andrew in view of Akiwumi-Assani.

Independent claims 9 and 17, as amended, also include limitations similar to those cited in claim 1, as amended. Thus, for reasons similar to those discussed above, it is respectfully submitted that claims 9 and 17, as amended, are patentable over Andrew in view Akiwumi-Assani.

Given that claims 4-8 depend from claim 1, as amended, claims 12-16 depend from claim 9, as amended and claims 20-24 depend from claim 17, as amended, for at least the reasons similar to those discussed above, it is respectfully submitted that claims 4-8, 12-16 and 20-24are patentable over the cited references:

CONCLUSION

In view of the foregoing, Applicant respectfully submits the present application is now in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call the undersigned attorney at (408) 720-8300.

Please charge Deposit Account No. 02-2666 for any shortage of fees in connection with this response.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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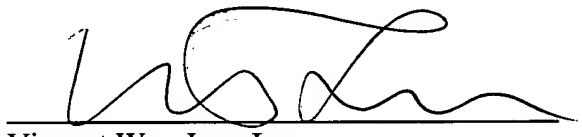

Vincent Wen Jeng Lue
Reg. No.: 56,564

12400 Wilshire Blvd.
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-8300